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Technical Bulletin

Design Considerations / Differences of MPC862SAR

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Section 1.0 Introduction

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The MPC860SAR and MPC862SAR are both members of the MPC8xx PowerQUICC™ family. In addition to the standard MPC860MH capabilities, the MPC860SAR and MPC862SAR include the universal test and operations physical PHY interface for ATM called UTOPIA. Both devices also provide AAL5 and AAL0, segmentation and re-assembly (SAR) functionality, an ATM pace controller (APC) and transmission convergence (TC) sub-layer for E1/DS1 and xDSL which is implemented by the serial channels.

In addition to these features, the allows the user to have simultaneous MII (Media Independent Interface) and UTOPIA capability while still maintaining backwards compatibility with the existing MPC860SAR controller.

These particular features make the 862SAR a very adaptable ATM SAR controller that can be used for a variety of ATM applications. Typical examples include:

- ATM line card controllers
- ATM to WAN interworking (frame relay, T1/E1 circuit emulation, xDSL applications)
- ATM25 applications.
- Residential broadband network interface units (ATM-to-Ethernet)
- High performance set-top controller.
- Bridging and routing applications.

The MPC862SAR is an enhanced version of the MPC860SAR. Although the MPC862SAR is pin compatible with both the MPC860 and MPC860SAR, a number of small, but significant programming changes have to be made to accommodate differences between the controllers.

The MPC857SART is a low cost derivative of the MPC862SAR including the same basic feature set with the exception that only 1 SCC is available to the user. Before selecting the MPC857SART as the host processor, careful consideration should be given as to whether the 1 SCC is capable of providing enough performance for the target application. In this instance, the use of the CPM PERFORMANCE SPREADSHEET given on the Motorola Netcomm web page at "http://www.mot.com/SPS/RISC/netcomm/tools/", is advised.

This document details the main differences in register and control bit settings that need to be taken into account when transitioning from the MPC8XXSAR to the Rev 0 MPC862SAR. The document references the "Enhanced SAR Functionality Supplement to the MPC860 PowerQUICC™ User's Manual" and the "MPC860 PowerQUICC™ User's Manual".

Both of these documents are available on the Motorola web site at the following URL: "http://www.mot.com/SPS/RISC/netcomm/docs/pubs/index.html".

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Section 2.0 ATM Enhancements

The MPC862 SAR has a number of additional features compared to the original MPC860 (Rev D and earlier revisions) of SAR. Table 1, below, details some of the additional features that the 862SAR processors can now support.

Table 1 – Main Functional Differences Between 860SAR & 862SAR

ATM Feature	MPC860SAR	MPC862SAR
Clock frequency UTOPIA interface.	≤ 25 MHz	≤ 50 MHz
Number of priority levels (APC)	2	Unlimited
Memory-memory cell processing?	Yes, Serial loopback only.	Yes, Serial or UTOPIA loopback
Port to Port switching ?	Yes, only with RAM microcode	Yes, no microcode needed!
Simultaneous MII & UTOPIA operation ?	No	Yes, when operating UTOPIA in muxed bus (Master) mode
ATM APC Queue Handler ?	No	** Yes, PTP queuing mechanism, flexible priority of queues
Backwards compatibility ?	Not applicable	Yes, through the ESAR bits
UTOPIA - Split Mode Capability (8-bit)	No – 8 Shared data signals only (Mux mode)	Yes – Mux mode + Split mode (2 separate 8 bit Rx & Tx buses in split mode).

*** See last paragraph of section 5.1 - Parameter RAM conflicts**
**** APC Queue errata – this feature is currently broken on Rev E.0.**

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Section 3.0 ATM Operational Differences

In order to highlight some of the operational differences between the 860SAR and the 862SAR, the reception and transmission of a typical ATM cell will be discussed for both processors.

3.1 ATM Cell Reception – 860SAR

1. Cell received from transmission line via UTOPIA interface and put into FIFO. When the RxClav signal (Receive Cell Available) is found to be asserted by the PHY, the SAR will receive a cell from that PHY.
2. Read cell header. In SAR mode, the UTOPIA is controlled by microcode that uses 4 byte long registers. Hence, when the RxClav is sent to the CPM, the cell is read in to the processor four bytes at a time.
3. Address Look-up. Match the header to get the correct channel number.
4. Get parameters from memory.
5. Read data from PHY UTOPIA interface to the CPM. This involved calculating the CRC (Cyclic Redundancy Check) and also sending out the relevant address to the DMA for memory access.
6. The relevant parameters in memory are updated - Buffer descriptor pointers, CRC counters etc.

3.2 ATM Cell Reception – 862SAR

1. Cell received from transmission line via UTOPIA interface and put into FIFO When the RxClav signal (Receive Cell Available) is found to be asserted by the PHY, the SAR will receive a cell from that PHY.
2. Read cell header. **In 862SAR, there is a UTOPIA hardware block that reads the entire cell into an internal 2 cell FIFO in a minimal amount of time. Hence, when the RxClav is sent to the CPM, the cell (n bytes) is read in to the processor within (n) clock cycles.**
3. Address Look-up. Match the header to get the correct channel number.
4. Get parameters from memory.
5. Read data from PHY UTOPIA interface to the CPM. This involved calculating the CRC (Cyclic Redundancy Check) and also sending out the relevant address to the DMA for memory access.
6. The relevant parameters in memory are updated i.e. Buffer descriptor pointers, counters etc.

The most noticeable difference between the 860SAR and 862SAR modes of operation is the actual implementation of how the whole cell is read into the CPM by the UTOPIA interface during cell reception. On the 860SAR, the UTOPIA interface is controlled by microcode. However, the 862SAR has a cell FIFO that is implemented by the UTOPIA hardware block and is independent from any microcode. This added 862SAR functionality requires some additional processing overheads although reading a cell takes a significantly shorter period of time on 862SAR compared to 860SAR.

For example, when the 860SAR reads a complete ATM cell of 53 bytes it takes between 300 – 500 CPM clock cycles depending on available bandwidth. The 862SAR, on the other hand, requires around 15-20% less clock cycles and is therefore much more efficient in terms of speed and bandwidth utilized.

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3.4 ATM Cell Transmission – 860SAR / 862SAR

The user-defined APC scheduler controls this process (assume IAQ bit is not set). The PHY will assert the TxClav signal (transmit cell available) when space is available in the PHY. If the APC is ready to transmit and space is available in the FIFO's, the cell is transmitted.

1. If a cell is available (TxClav is asserted) and the APC scheduler is ready to transmit, then the channel number is read from the APC transmit queue.
2. Read channel parameters – buffer descriptors, counters etc.
3. Transmit header. If the cell to be transmitted is an AAL5 cell then the information resides in connection tables and parameter RAM. If the cell to be transmitted is an AAL0 cell then the information resides in memory.
4. Transmit payload. This includes direct memory access (DMA) from the buffers with optional cyclic redundancy check (CRC).
5. Update parameters – parameter table entries.

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Section 4.0 Programming Considerations

In order to take advantage of the new features contained on the 862SAR device, a number of significant programming considerations must be taken into account. This is often a fundamental cause of many 860SAR/862SAR software bugs.

- SCC Parameter RAM. Page 4 of this memory area contains all of the necessary connection tables, buffer descriptors and data buffers required for 862SAR operation. Hence, this section of memory **MUST** be cleared during the initialization sequence prior to any 862SAR operation otherwise the 862SAR may not operate / may operate unpredictably.

- In order to enable backwards compatibility i.e. perform 860SAR functionality using 862SAR silicon, **ALL** ESAR bits must be cleared through the ESAR register set. The reason for this is to reduce the complexity of the internal microcode. Thus, the ESAR bits in registers SRSTATE, STSTATE, APCST should all be cleared. Similarly, if 862SAR functionality is required these bits should be set in all of the above registers.

- The 862SAR device allows the user to program or modify any memory location on the fly without conflicting with the current CPM process. It is only possible to do this using the WRITE_TO_MEMORY command. Attempting to modify any memory location without using this command will cause system CPM failure. [Adding / removing internal channels and modifying the APC period can also be changed on-the-fly in both 860SAR and 862SAR modes. Consult the supplementary 862SAR documentation at the following URL "http://www.mot.com/SPS/RISC/netcomm/docs/pubs/index.html", for further details].

- Customers should also be aware of a possible required software change in transitioning from the MPC862SAR Rev 0 to Rev A when using the Port–to–Port functionality.

  In Rev 0, customers should ensure that the **TB_PTR** field inside any TCT (transmit connection table) used for PTP (Point to Point connections) are initialised in the following manner:

  The upper 16 bits (starting at offset 0x08 in the TCT) must be set to the same value as the receive buffer descriptor base pointer value (RBD_PTR). The lower 16 bits (starting at offset 0x0A in the TCT) must be cleared. This change will allow compatibility between revisions 0 and A. Software that is not initialised in this manner for Port-to-Port applications may exhibit erratic behaviour.

- Customers planning to use silicon Rev A should avoid writing non-zero values to the 32 bit location IMMR+0x3CB8, even for non-ATM applications, unless specifically required by Motorola. Rev A will reserve this location for internal CPM usage.

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Section 5.0 862SAR Mode - Internal Resource Conflicts

When operating an ATM application in 862SAR mode, the MPC862SAR loses some functionality due to internal resource conflicts. The following section details potential restrictions and conflicts that can arise.

5.1 Parameter RAM Conflicts

As 862SAR mode requires additional memory, users should be aware of the potential conflicts that can occur in parameter RAM. If operating in serial ATM mode on SCC1-4 or UTOPIA on SCC4, this will cause other peripherals to lose their parameter RAM. The serial ATM parameters of SCC1 extend into the I^2C parameter RAM. Similarly, the parameter RAM for SCC2/SPI, SCC3/SMC1 and SCC4/SMC2/PIP is affected in the same manner.

In order to relocate the parameter RAM for the SMC's, I^2C and SPI controllers to a non-conflicting location, RAM- based microcode patches can be used. These microcode patches are available on the Motorola MPC8xx website - http://www.mot.com/SPS/RISC/netcomm/tools/". (On MPC862 the relocation of the I2C/SPI does not require a RAM microcode patch. the device contains the relocatable I2C/SPI functionality and works as described in the pdf for the RAM loadable microcode of previous revisions.)

[On MPC862 Rev 0, a current bug in the implementation of the microcode means that when RAM microcodes are enabled, all information in the ROM microcode is lost at locations >=0x2000. The net result is that ATM functionality of the device is effectively lost. Currently no workaround exists although this bug should be resolved on silicon revision A.]

5.2 IDMA2 Conflicts

IDMA2 can only be used in level-sensitive mode when ATM is enabled. In order to achieve this mode, the user is required to set the RCCR[DR1M] bit.

5.3 UTOPIA Conflicts

The UTOPIA interface is implemented using the hardware of IDMA1 and the parameter RAM page of SCC4. Therefore, if the UTOPIA port is used:

- SCC4 is unavailable due to the loss of parameter RAM page 4.
- IDMA1 is unavailable. (The DREQ0 signal is lost, and the IDMA1 event and mask registers IDSR1 and IDMR1 are used for UTOPIA events.)
- Ethernet CAM support for SCC2, SCC3, and SCC4 is unavailable (due to the loss of REJECT2, REJECT3, and REJECT4)
- Parallel interface port (PIP) is unavailable (due to the loss of the PIP handshake signals)

The UTOPIA interface can also be made to operate in either UTOPIA split bus mode of operation or using master mode operation. Depending on initial register programming, specific port pin functions become available or unavailable to the user:

In 862SAR multi-PHY mode:

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- In UTOPIA split bus mode, PCMCIA port A and the Fast Ethernet controller's (FEC) MII signals are unavailable. However in UTOPIA muxed bus mode, the MII signals or the PCMCIA port A signals are still available on the PCMCIA port A pins.

  In 862SAR multi-PHY mode:

- The PHY address signals conflict with the signals of both SMCs. However, when a PHY address signal is not activated, the pin's other signal functions become available. For example, if only eight PHYs are used in a UTOPIA master application, the SMC1 data signals are still available.

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Section 6.0 Pin Assignment Comparison Between MPC860 & MPC862SART

The table below illustrates the pin assignment differences between the MPC860 and the MPC862SART. The Italic text displayed in green indicates 862SAR specific modes of operation.

PIN NAME	*COMMENTS*	*PIN NAME*	*COMMENTS*
A2 CS1			
A3 CE2_A/*MII-TXD3*	*862SAR Simultaneous MII / UTOPIA operation.*	**B1** UPWAITB/GPL_B4	
A4 CS4		**B2** RD/WR	
A5 WE3/BS_B3/PCWE		**B3**CE1_A/*MII-TXD2*	*862SAR Simultaneous MII / UTOPIA operation.*
A6 WE1/BS_B1/IOWR		**B4** CS5	
A7 BS_A2		**B5** GPL_A2/GPL_B2/CS2	
A8 VDDL		**B6** WE2/BS_B2/PCOE	
A9 A31		**B7** MII_CRS	
A10 A28		**B8** BS_A3	
A11 A30		**B9** TSIZ0/REG	
A12 A29		**B10** A22	
A13 A27		**B11** A23	
A14 A14		**B12** A21	
A15 A11		**B13** A17	
A16 A7		**B14** A13	
A17 A5		**B15** A10	
A18 A2		**B16** A6	
		B17 A4	
		B18 A1	
		B19 A0	
C1 UPWAITA/GPL_A4		**D1** TEA	
C2 TA		**D2** BDIP/GPL_B5	
C3 CS0		**D3** GPL_A5	
C4 CS7/CE(2)B		**D4** CS2	
C5 GPL_A3/GPL_B3/CS3		**D5** CS6/CE(1)B	
C6 OE/GPL_A1/GPL_B1		**D6** N/C	
C7 WE0/BS_B0/IORD		**D7** GPL_A0/GPL_B0	
C8 BS_A1		**D8** BS_A0	
C9 TSIZ1		**D9** A18	
C10 A26		**D10** A25	
C11 A24		**D11** A19	
C12 A20		**D12** A15	
C13 A16		**D13** N/C	
C14 A12		**D14** N/C	
C15 A9		**D15** A8	
C16 A3		**D16** PC[15]/DREQ0/RTS1/L1ST1/Rxclav	
C17 PB[31]/REJECT1/SPISEL		**D17** PA[14]/TXD1	
C18 PA[15]/RXD1		**D18** PC[14]/DREQ1/L1ST2	

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C19 PB[30]/SPICLK/RSTRT2		**D19**PB[28]/SPIMISO/BRGO4	
E1 BB		**F1** BURST	
E2 BG		**F2** CR/IRQ3	
E3 BI		**F3** TS	
E4 CS3		**F4** VDDH	
E5 VDDH		**F5** VDDH	
E6 VDDH		**F6** GND	
E7 VDDH		**F7** GND	
E8 VDDH		**F8** GND	
E9 VDDH		**F9** GND	
E10 VDDH		**F10** GND	
E11 VDDH		**F11** GND	
E12 VDDH		**F12** GND	
E13 VDDH		**F13** GND	
E14 VDDH		**F14** GND	
E15 VDDH		**F15** VDDH	
E16 PB[29]/SPIMOSI		**F16** VDDH	
E17 PA[13]		**F17** PA[12]	
E18 PC[13]/L1RQB/L1ST3		**F18** PC[12]/L1RQA/L1ST4	
E19 PB[27]/I2CSDA/BRGO1		**F19**PB[26]/I2CSCL/BRGO2	
G1 IP_B3/IWP2/VF2		**H1** IP_B7/PTR/AT3	
G2 IP_B4/LWP0/VF0		**H2** IP_B0/IWP0/VFLS0	
G3 FRZ/IRQ6		**H3** RSV/IRQ2	
G4 BR		**H4** MII_COL	
G5 VDDH		**H5** VDDH	
G6 GND		**H6** GND	
G7 GND		**H7** GND	
G8 GND		**H8** GND	
G9 GND		**H9** GND	
G10 GND		**H10** GND	
G11 GND		**H11** GND	
G12 GND		**H12** GND	
G13 GND		**H13** GND	
G14 GND		**H14** GND	
G15 VDDH		**H15** VDDH	
G16 PA[11]/L1TXDB		**H16** TCK/DSDK	
G17 TDO/DSDO		**H17** TDI/DSDI	
G18 TMS		**H18** MII_MDIO	
G19 TRST		**H19** VDDL	
J1 ALE_B/DSCK/AT1		**K1**KR/IRQ4/RETRY/SPKROUT	
J2 IP_B2/IOIS16_B/AT2		**K2** ALE_A/*MII-TXD1*	*862SAR Simultaneous MII / UTOPIA operation*
J3 IP_B1/IWP1/VFLS1		**K3** IP_B6/DSDI/AT0	
J4 IP_B5/LWP1/VF1		**K4** BADDR30/REG	
J5 VDDH		**K5** VDDH	
J6 GND		**K6** GND	
J7 GND		**K7** GND	
J8 GND		**K8** GND	
J9 GND		**K9** GND	

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J10 GND		**K10** GND	
J11 GND		**K11** GND	
J12 GND		**K12** GND	
J13 GND		**K13** GND	
J14 GND		**K14** GND	
J15 VDDH		**K15** VDDH	
J16PB[25]/SMTXD1/*RXADDR3 / TXADDR3*	*862SAR Multi-PHY mode operation only*	**K16**PB[21]/SMTXD2/L1CLKOB/*TXADDR1/ RXADDR1*	*862SAR Multi-PHY mode operation only*
J17 PA[10]/L1RXDB		**K17**PB[23]/SMSYN1/SDACK1/*TXADDR2/ RXADDR2*	*862SAR Multi-PHY mode operation only*
J18PB[24]/SMRXD1/*TXADDR3 /RXADDR3*	*862SAR Multi-PHY mode operation only*	**K18** PA[9]/L1TXDA	
J19 PC[11]/CTS1		**K19** PC[10]/CD1/TGATE1	
L1 MODCK1/OP2/STS		**M1** VDDL	
L2 OP1		**M2** BADDR29	
L3 AS		**M3** BADDR28	
L4 OP0/*MII-TXD0/UtpClk_Aux*	*862SAR Simultaneous MII / UTOPIA split bus operation.*	**M4**OP3/MODCK2/DSDO	
L5 VDDH		**M5** VDDH	
L6 GND		**M6** GND	
L7 GND		**M7** GND	
L8 GND		**M8** GND	
L9 GND		**M9** GND	
L10 GND		**M10** GND	
L11 GND		**M11** GND	
L12 GND		**M12** GND	
L13 GND		**M13** GND	
L14 GND		**M14** GND	
L15 VDDH		**M15** VDDH	
L16PB[20]/SMRXD2/L1CLKOA /*TXADDR0/RXADDR0*	*862SAR Multi-PHY mode operation only*	**M16**PC[7]/L1TSYNCB/SDACK2	
L17 PA[8]/L1RXDA		**M17** PA[6]/BRGCLK1/TOUT1/CLK2	
L18 PC[9]		**M18** PC8/TGATE2	
L19PB[22]/SMSYN2/SDACK2/ *TXADDR4/RXADDR4*	*862SAR Multi-PHY mode operation only*	**M19**PA[7]/CLK1/TIN1/L1RCLKA/BRGO1	
N1 EXTAL		**P1** XTAL	
N2 EXTCLK		**P2** SRESET	
N3 TEXP		**P3** RSTCONF	
N4 HRESET		**P4** VDDH	
N5 VDDH		**P5** VDDH	
N6 GND		**P6** GND	
N7 GND		**P7** GND	
N8 GND		**P8** GND	
N9 GND		**P9** GND	
N10 GND		**P10** GND	
N11 GND		**P11** GND	
N12 GND		**P12** GND	
N13 GND		**P13** GND	
N14 GND		**P14** GND	
N15 VDDH		**P15** VDDH	

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N16 PB[16]/L1RQA/L1ST4/*TXADDR0/RXADDR0*	*862SAR Multi-PHY mode operation only*	**P16** VDDH	
N17 PB[18]/L1ST2/RTS2/*RXADDR4/TXADDR4*	*862SAR Multi-PHY mode operation only*	**P17**PA[3]/CLK5/TIN3/BRGOUT3	
N18 PA5/CLK3/TIN2/L1TCLKA/BRGOUT2		**P18**PB[17]/L1RQB/L1ST3/*TXADDR1/RXADDR1*	*862SAR Multi-PHY mode operation only*
N19 PB[19]/L1ST1/RTS1		**P19** PA[4]/TOUT2/CLK4	
R1 KAPWR		**T1** VDDSYN	
R2 PORESET		**T2** XFC	
R3 WAIT_A/*SOC_Aux*	*862SAR Simultaneous MII / UTOPIA split bus operation.*	**T3**IP_A7/*UTPB_Aux7/MII-RXDV*	*862SAR Simultaneous MII / UTOPIA operation.*
R4 WAIT_B		**T4**IP_A1/*UTPB_Aux1/MII-RXD2*	*862SAR Simultaneous MII / UTOPIA operation.*
R5 VDDH		**T5**IP_A0/*UTPB_Aux0/MII-RXD3*	*862SAR Simultaneous MII / UTOPIA operation.*
R6 VDDH		**T6**IP_A6/*UTPB_Aux6/MII-TX-ERR*	*862SAR Simultaneous MII / UTOPIA operation.*
R7 VDDH		**T7** D31	
R8 VDDH		**T8** D25	
R9 VDDH		**T9** D22	
R10 VDDH		**T10** D15	
R11 VDDH		**T11** D9	
R12 VDDH		**T12** D17	
R13 VDDH		**T13** D12	
R14 VDDH		**T14** VDDH	
R15 VDDH		**T15** PD[7]/MII-RX-ERR/UTPB4	
R16 PD[12]/L1RSYNCB/*MII-MDC/UTPB3*	*Available only in simultaneous MII & UTOPIA operation*	**T16** PD[11]/*MII-TX-ERR RXD3/RXENB*	*Available only in simultaneous MII & UTOPIA operation*
R17 PB[15]/BRGO3/Txclav		**T17** PC[4]/L1RSYNCA	
R18PA[2]/CLK6/TOUT3/L1RCLKB/BRGCLK2		**T18**PC[5]/L1TSYNCA/SDACK1	
R19 PC[6]/L1RSYNCB		**T19** PA[1]/CLK7/TIN4/BRGO4	
U1 VSSSYN		**V1** VSSSYN1	
U2 N/C		**V2** N/C	
U3IP_A2/IOIS16_A/*UTPB_Aux2/MII-RXD1*	*862SAR Simultaneous MII / UTOPIA operation.*	**V3** DP0/IRQ3	
U4IP_A4/*UTPB_Aux4/MII-RXCLK*	*862SAR Simultaneous MII / UTOPIA operation.*	**V4** DP3/IRQ6	
U5IP_A5/*UTPB_Aux5/MII-RX-ERR*	*862SAR Simultaneous MII / UTOPIA operation.*	**V5** DP1/IRQ4	
U6 D30		**V6** D28	
U7 D26		**V7** D24	

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U8 D21		**V8** D20	
U9 D19		**V9** D18	
U10 D16		**V10** D14	
U11 D11		**V11** D10	
U12 D23		**V12** D27	
U13 D8		**V13** D13	
U14 IRQ1		**V14** IRQ0	
U15 PD[5]/*MII-TXD3*/REJECT2/UTPB6	*Available only in simultaneous MII & UTOPIA operation*	**V15** MII_TX_EN	
U16 PD[4]/*MII-TXD2*/REJECT3/UTPB7	*Available only in simultaneous MII & UTOPIA operation*	**V16** PD[6]/*MII-RXDV*/RTS4/UTPB5	*Available only in simultaneous MII & UTOPIA operation*
U17PD[15]/L1TSYNCA/*MII-RXD3*/UTPB0	*Available only in simultaneous MII & UTOPIA operation*	**V17** PD[9]/*MII-TXD0*/RXD4/UTPCLK	*Available only in simultaneous MII & UTOPIA operation*
U18PB[14]/RSTRT1/*RXADDR2*		**V18**PD[13]/L1TSYNCB/*MII-RXD1*/UTPB2	*Available only in simultaneous MII & UTOPIA operation*
U19PA[0]/CLK8/TOUT4/L1TCLKB		**V19**PD[14]/L1RSYNCA/*MII-RXD2*/UTPB1	*Available only in simultaneous MII & UTOPIA operation*
W2IP_A3/UTPB_Aux3/MII-RXD0	862SAR Simultaneous MII / UTOPIA operation.		
W3 CLKOUT			
W4 DP2/IRQ5			
W5 D29			
W6 D7			
W7 D6			
W8 VDDL			
W9 D5			
W10 D3			
W11 D2			
W12 D1			
W13 D4			
W14 D0			
W15 IRQ7/MII_TXCLK			
W16 PD[3]/MII-TXD1/SOC			
W17 PD[8]/TXD4/*MII-RX_CLK/MII-MDC*	*Available only in simultaneous MII & UTOPIA operation*		
W18 PD[10]/TXD3/MII-RXD0/TXENB	*Available only in simultaneous MII & UTOPIA operation*		

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7.0 Register Comparison Between 860SAR & 862SAR

The following spreadsheets detail the differences between 860SAR and 862SAR throughout the register set of the MPC8XX:

Connection Tables - SAR vs ESAR

Receive Function Code & Status Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field				BO		FC			EXT	ACP	EC*	SNC*	ESAR	MCF	SER	MPHY *

ESAR — Must also be set to enable ESAR functionality

MCF — Enable management cell filter

* Available only in SCC4 UTOPIA mode; otherwise written as 0

Transmit Function Code & Status Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field				BO		FC			EXT		EC*	SNC*	ESAR		SER	MPHY *

ESAR — Must also be set to enable ESAR functionality

* Available only in SCC4 UTOPIA mode; otherwise written as 0

APC Status Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field		CSER		NSER		*			**				ESAR	DIS	PL2***	MHY

ESAR	Must also be set to enable ESAR functionality
*	Was NMPHY on SAR, now bits [2.6] in MPHY status register on ESAR
**	Was CMPHY on SAR, now bits [10.14] in MPHY status register on ESAR
PL2***	Used only if ESAR is not set for backwards compatibility with the MPC860SAR

MPHY Status Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field					NMPHY								CMPHY			

NMPHY	Number of Multiple PHY's
CMPHY	Current Multiply PHY

CPM Command Register

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	RST	ATM OPCODE			OPCODE=1111				CH_NUM					OPCODE 2		FLG

ATM OPCODE OPCODE 2	111 = ATM ESAR Write to Memory Command or internal command (see OPCODE 2) 00 = RESERVED, normal ATM OPCODES apply when 00 is written to these two bits 01 = ACTIVATE PM - to activate PM session on the channel number specified by the COMM_CH field. * 10 = DEACTIVATE PM - To deactivate PM session on the channel number specified by the COMM_CH field. * 11 = RESERVED * OPCODE 2 commands are only valid when ATM OPCODE=111

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ESAR APC Status Register (From APC Parameter RAM)

Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	APCOM	*	LAST	*								EQ	ESAR	DIS	*	MPHY

*	Reserved
APCOM	APC table overrun event mask for this APC level.
LAST	This priority level is the last APC level for the specific PHY#.
EQ	APC table and PTP queue of this specific level have equal priority. The APC mechanism will schedule cells to be transmitted evenly from the two utilities. This bit is valid only if the DIS bit is NOT set.
ESAR	Selects the new features of ESAR or allows backward compatibility with the older SAR functionality. To enable ESAR functionality, all bits must be programmed to the desired value throughout the ESAR register set.
DIS	APC table is disabled at this level. PTP queue will still be serviced. All lower levels down to LAST will still be serviced. Can only be set on the fly using the “write to memory” command (Page 4-22 of ESAR spec) to avoid conflict.
MPHY	All M-PHY bits (throughout the ESAR register set) should be set to desired values when working with multi-PHY.

UTOPIA Mode Event Register

Base	0	1	2	3	4	5	6	7
Field				SYNC	IQOV	GINT	GUN	GOV

GUN	Global transmitter underrun in UTOPIA's tx cell FIFO.
GOV	Global receiver underrun in UTOPIA's rx cell FIFO.

Interrupt Queue Entry

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Base	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	W		CNG					APC0		TQF	UN	RXF	BSY	TXB	RXB
	Transmit queue full - this bit is valid in case that an APC bypass command was issued and the Transmit queue is full, indicating that the APC bypass command was noperformed.This bit is valid only for AAL0 PTP channels where ITQ option is set.														

Performance Monitoring

Section 4.3 covers this new feature for ESAR. Correct configuration is achieved by programming table 4-2.

Connection Tables - SAR vs ESAR

Receive Connection Table - RCT

Base	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CT_Offset + 0	FHNT							HEC	CLP	CNG/NCRC	INF	CNGI/PTP	CDIS	AAL	
	PM NCRC PTP	Performance Monitoring No CRC (AAL0 only) / Congestion (AAL5 only) Port to Port cell switching / Congestion interrupt (AAL5 only)													
CT_Offset + 2	RBALEN														
CT_Offset + 4	RCRC														
CT_Offset + 6															
CT_Offset + 8	RB_PTR														
CT_Offset + A															
CT_Offset + C	RTMLEN														
CT_Offset + E	RBD_PTR														
CT_Offset + 10	RBASE														

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CT_Offset + 12	TSTAMP														
CT_Offset + 14	AAL2	IMASK													
	AAL2	Indicates this VC is an AAL2 channel. Must initialise prior to setting !													
CT_Offset + 16	FT	NIM			RPMT										
	FT	Filter Type													
	NIM	Non intrusive monitoring													
	RPMT	Receive performance monitoring table number													
CT_Offset + 18 to CT_Offset + 1F	Reserved														

Port to Port Specific Receive Connection Table - PTP RCT

When PTP function is used a new RCT must be defined called PTP RCT.
It is a specific RCT which must be initialized as page 2-15. All of the fields are new.

Transmit Connection Table - TCT

Base	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CT_Offset + 20								PC			INF	CR10	CDIS	AAL	
	PM	Performance Monitoring													
CT_Offset + 22	TBALEN														
CT_Offset + 24	TCRC														
CT_Offset + 26															
CT_Offset + 28	TB_PTR														
CT_Offset + 2A															
CT_Offset + 2C	TTMLEN														
CT_Offset + 2E	TBD_PTR														
CT_Offset + 30	TBASE														
CT_Offset + 32					TPMT									AVCF	ACT
	TPM	Transmit Performance monitoring table number													

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	T AVC F ACT	Auto VC off Active Statu s
CT_Offset + 34 CT_Offset + 36	CHE AD	
CT_Offset + 38	APCL	
CT_Offset + 3A	APC PR	
CT_Offset + 3C	OUT	TSE R / APC P
	BNR TSER VICE: APC P	Buffer Not Ready (Internal Use) Traffic service type APCP <= 4094 instead of 32766 in SAR
CT_Offset + 3E	APC PF	

Transmit connection Table Extensions TCTE

Located at TCTEBASE programmed in Parameter RAM, the TCTE are located in DPRAM.
They support VBR channels to hold additional parameters for traffic shaping.

Buffer Descriptors - SAR vs ESAR

Receive Buffer Descriptor

Base	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Offset + 0	E	W	I	L	F/OAM	CM	FMC	HEC	CLP	CNG	ABT			LN	CR
	F/OAM	F (AAL5) First in Frame. OAM (AAL0) Operation and Maintenance cell indication.													
	FMC	Forward Monitoring Cell received + BRC fields added													
Offset + 2	DATA LENGTH / Channel Code														
	Data length	Number of bytes written into BD's data buffer (AAL5)													
	Channel	Channel number when AAL0 buffers + MCF bit set													

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	Code
Offset + 4	RX DATA BUFFER POINTER
Offset + 8	CPCS-UU+CPI
Offset + A	RESERVED
Offset + C	CELL HEADER EXPANSION 1
Offset + 10	CELL HEADER EXPANSION 2
Offset + 14	CELL HEADER EXPANSION 3

Transmit Buffer Descriptor

Base	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Offset + 0	R	W	I	L	OAM	CM							ICNG	RH	ICLP
	OAM	User Cell / Non User Cell													
	ICNG	Invert CNG bit (AAL5 only)													
	RH	Replace header (AAL5 only)													
	ICLP	Invert CLP bit (AAL5 only)													
Offset + 2	DATA LENGTH														
Offset + 4	TX DATA BUFFER POINTER														
Offset + 8	CPCS-UU+CPI/HEADER_L														
	HEADER_L	Lower half word of the replacement header													
Offset + A	Reserved/HEADER_H														
	HEADER_H	Upper half word of the replacement header													
Offset + C	CELL HEADER EXPANSION 1														
Offset + 10	CELL HEADER EXPANSION 2														
Offset + 14	CELL HEADER EXPANSION 3														

Parameter RAM Mapping - SAR vs ESAR

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Serial and Utopia Interface Parameter RAM Map

Offset from SCC Base	Name	Description	SAR Function	ESAR Function
0x00	RBDBASE	Base pointer for receiveBDs		
0x04	SRFCR/SRSTATE	SAR receive function code and receive status	SRFCR/SRSTAE[12] does not exist SRFCR/SRSTAE[13]= DIS Disable Utopia receive process	SRFCR/SRSTAE[12]= ESAR bit Enable ESAR functions SRFCR/SRSTAE[13]= MCF Enable management cell filter
0x06	MRBLR	Maximum receive buffer length		
0x08	RSTATE	SCC internal receive state parameters		
0x0C	Reserved			
0x10	R_CNT	Receive internal byte counter		
0x12	STFCR/STSTATE		STFCR/STSTATE[9] = TQF Transmit Queue Full in 850SAR STFCR/STSTATE[9] = Reserved in 860SAR until Rev C1 STFCR/STSTATE[9] = TQF Transmit Queue Full in 860SAR in Rev D STFCR/STSTATE[11] = PBF Port B Flag STFCR/STSTATE[12] = Reserved	850 ESAR doesn't exist STFCR/STSTATE[9] = Reserved STFCR/STSTATE[9] = Reserved STFCR/STSTATE[11] = Reserved STFCR/STSTATE[12] = ESAR Enable ESAR functions
0x14	TBDBASE	Base pointer for transmitBDs		
0x18	TSTATE	SCC internal transmit state parameters		
0x1C	COMM_CH	Command channel		
0x1E	STCHNUM	Current transmit channel number		
0x20	T_CNT	Transmit internal byte counter		
0x22	CTBASE	Connection table base address		
0x24	ECTBASE	External connection table base address		
0x28	INTBASE	Interruput base pointer		
0x2C	INTPTR	Pointer to interrupt queue		
0x30	C-MASK	Constant mask for CRC32		
0x34	SRCHNUM	Current receive channel number		
0x36	INT_CNT	Interrupt counter		

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0x38	INT_ICNT	Interrupt initial value		
0x3A	TSTA	Time stamp timer address		
0x3C	OLDLEN	Transmitter temporary length		
0x3E	SMRBLR	SAR maximum receive buffer length register		
0x40	EHEAD	Empty cell header		
0x44	EPAYLOAD	Empty cell payload		
0x48	TQBASE	Transmit queue base pointer		TQBASE: Reserved in MPHY mode
0x4A	TQEND	Transmit queue end pointer		TQEND: Reserved in MPHY mode
0x4C	TQAPTR	Transmit queue APC pointer		TQAPT: Reserved in MPHY mode
0x4E	TQTPTR	Transmit queue transmitter pointer		TQTPTR: Reserved in MPHY mode
0x50	APCST	APC status Number of multiple PHY Current Multi PHY Utopia Level 2 MPHY Priority table Level 2	 APCST[5-7] = NMPHY APCST[8-10] = CMPHY APCST[12] = Reserved APCST[14] = PL2	 APCST[5-7] = Reserved Reserved if ESAR bit in APCST = 1 APCST[8-10] = Reserved Reserved if ESAR bit in APCST = 1 APCST[12] = ESAR APCST[14] = PL2 Reserved if ESAR bit in APCST = 1
0x52	APCPTR	APC parameter pointer		MPHY master: Points to MPHY pointing table
0x54	AM1	Address match parameter		
0x56	AM2	Address match parameter		
0x58	AM3	Address match parameter		
0x5A	AM4	Address match parameter		
0x5C	AM5	Address match parameter		
0x5E	ECSIZE	Expanded cell size/unassigned cell data		ECSIZE: new configuration
0x60	APCT_REAL	APC 32 bit counter		Used internally by the APC for VBR traffic. Must be initialised to zero.
0x64	R_PTR	Receiver internal data pointer		
0x68	RTEMP	Receiver temporary data storage		
0x6C	T_PTR	Transmit internal data pointer		
0x70	TTEMP	Transmitter temporary data storage		
0x74 to 0x7F	Reserved			

ESAR

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Parameters

Offset from SCC Base	Name	Description	SAR Function	ESAR Function
0x80	FMCTIMESTMP	OAM performance monitoring time stamp counter address	Doesn't exist	
0x84	FMCTEMPLATE	OAM performance monitoring - FMC template pointer	Doesn't exist	
0X88	PMPTR	OAM performance monitoring table pointer	Doesn't exist	
0x8A	PMCCHANNEL	Temporary storagecountaning pmchannel number	Doesn't exist	
0x8C	Reserved		Doesn't exist	
0x90	MPHYST	MultiPHY status	Doesn't exist	
0x92	TCTEBASE	Internal TCT extension base	Doesn't exist	
0x94	ETCTEBASE	External TCT Extension Base pointer	Doesn't exist	
0x98	COMM_CH2	Second host command channel / MSB = 0x0000	Doesn't exist	
0x9C	STATBASE	Statistics table base pointer	Doesn't exist	
0x9C to 0xBF	Reserved			

Serial Interface Parameter RAM Map

Offset from SCC Base	Name	Description	SAR Function	ESAR Function
0xC0	ALPHA	Receiver delineation alpha/delta counters		
0xC2	DELTA	Receiver delineation alpha/delta counters		
0xC4	RSTUFF	Receive data stuffing location		
0xC8	SHUFFLESTATE	Receiver data shuffling state		
0xCA	RHECTEMP	Receiver temporary HEC storage area		
0xCC	THECTEMP	Transmitter temporary HEC storage area		
0xCE	ASTATUS	Cell synchronization status register		
0xD0	HEC_ERR	HEC error counter		
0xD2	Reserved			
0xD4	RSCRAM	Receiver scrambling storage		
0xD8	RSCRAM1	Receiver scrambling storage		
0xDC	TSCRAM	Transmitter scrambling storage		
0xE0	TSCRAM1	Transmitter scrambling storage		
0xE4	RCRC	Receiver temporary CRC		
0xE8	TCRC	Transmitter temporary CRC		

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0xEC	RCHAN	Receiver current channel		
0xF0	TCHAN	Transmitter current channel		
0xF4 to 0xFF	Reserved			

APC Parameter RAM Map

Offset from APCPTR	Name	Description	SAR Function	ESAR Function
0x00	APCT_BASE1	APC table first priority base pointer		
0x02	APCT_END1	First APC table length		
0x04	APCT_PTR1	First APC pointer		
0x06	APCT_SPTR1	First APC priority service pointer		
0x08	ETQBASE	Enhanced Transmit Queue base pointer		
0x0A	ETQEND	Enhanced Transmit Queue end pointer		
0x0C	ETQAPTR	Enhanced Transmit Queue APC pointer		
0x0E	ETQTPTR	Enhanced Transmit Queue transmitter pointer		
0x10	APC_MI	APC - Maximum iteration		
0x12	NCITS	Number of cells in time slot		
0x14	APCNT	APC - N timer		
0x16		Reserved		
0x18	EAPCST	APC status of the first priority service		
0x1A	PTP COUNTER	First priority PTP queue length		
0x1C	PTP_TxCH	First priority PTP channel		
0x1E		Reserved		
* * * * *				
(n * 0x20) + 0x0	APCT_BASEn	APC table—N'th priority table base pointer		
(n * 0x20) + 0x2	APCT_ENDn	N'th table —Length		
(n * 0x20) + 0x4	APCT_PTRn	N'th APC table pointer		

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(n * 0x20) + 0x6	APCT_SPTRn	N'th table APC service pointer		
(n * 0x20) + 0x8 -> +0x17		Reserved		
(n * 0x20) + 0x18	EAPCSTn	APC status of the N'th priority service		
(n * 0x20) + 0x1C	PTP_COUNTERn	N'th priority PTP queue length.		
(n * 0x20) + 0x1E		Reserved		

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